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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/820,243	03/28/2001	Terry L. Kendall	42390P10070	3769

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD, SEVENTH FLOOR
LOS ANGELES, CA 90025

EXAMINER
PORTKA, GARY J

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 09/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/820,243	Kendall
Examiner	**Art Unit**
Gary J. Portka	2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *March 28, 2001; July 2, 2001* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-20* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *Jul 2, 2001* is/are a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. The Office acknowledges receipt of the following:

   a. Executed Declaration, dated July 2, 2001.

2. Claims 1-20 are presented for examination.

Specification

3. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. The disclosure is objected to because of the following informalities:

   a. Claim 11 is objected to at line 2, "said" should be entered before "determining" for clarity.

   Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 1-3, 6-8, 10-11, and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Taylor et al., U.S. Patent 6,263,398 B1.

7. As to claims 1-3 and 6-8, Taylor discloses the recited memory with cache, integrated, and flash (see Abstract, Figure 1, and column 3 lines 7-35).

8. As to claims 10-11 and 15, Taylor discloses the flash memory and cache on same integrated circuit as described above. The method regarding requesting data via address compare and retrieving from the cache or memory to requester and cache is disclosed also (see Figure 1 at item 24, Figure 6, particularly at items 508 and 514, and column 9 line 31 to column 10 line 22).

9. Claims 1-2, 6-7, and 10-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Sakamoto, U.S. Patent 6,288,923 B1.

10. As to claims 1-2 and 6-7, Sakamoto discloses the recited memory with cache, integrated (see Abstract, Figure 2, column 1 line 57 to column 2 line 8).

11. As to claims 10-11, Sakamoto disclosed the memory and cache on same integrated circuit as described above. The method regarding requesting data via address compare and retrieving from the cache or memory to requester and cache is disclosed also (see Figures 5A to 5E, and column 6 lines 1-55).

12. As to claims 12-13, Sakamoto discloses quadword retrieval, as is apparent from Figures 6-10.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary

skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto, U.S. Patent 6,288,923 B1, or alternatively over Taylor et al., U.S. Patent 6,263,398 B1.

15. As to claim 5, neither Sakamoto nor Taylor disclose integrating the memory and cache with the processor. However, each teaches benefits of integrating in general (may lower costs and improve performance); such benefits are notoriously well known in the art and likewise well known to be scalable. Examiner takes Official Notice that an artisan would have known that integrating memory and cache with processor might provide like benefits and would have thus desired to do so. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to integrate memory, cache, and processor, because integration is scalable and the benefits thereof were well known.

16. Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto, U.S. Patent 6,288,923 B1, in view of the admitted prior art.

17. As to claims 16-18, Sakamoto discloses burst request, determining if addresses are in cache integrated with memory, and retrieving from cache or from memory to cache, and initiating transfer to requester (see Abstract, Figure 2, Figures 5A to 5E, column 1 line 57 to column 2 line 8, and column 6 lines 1-55). Sakamoto does not disclose interrupting and then resuming the transfer. However, this has been admitted as prior art by Applicants at page 9 lines 1-5. An artisan would have desired to interrupt and then resume in order to more quickly process a higher priority transfer, as admitted known in the art by Applicants. Thus it would have been obvious to one of ordinary skill

in the art at the time of the invention to interrupt and then resume transfer, because this was known in the art to allow faster processing of higher priority transfers.

18. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto, U.S. Patent 6,288,923 B1, in view of the admitted prior art, and further in view of Taylor et al., U.S. Patent 6,263,398 B1.

19. As to claim 19, neither Sakamoto nor the admitted prior art disclose the memory is flash. However, as taught by Taylor the benefits of non-volatility may be gleaned by using a flash integrated with a cache similarly to the device of Sakamoto (see Taylor Abstract, column 3 lines 7-14). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use flash in Sakamoto, because this was known in integrated memory/cache devices to achieve non-volatility.

20. Claims 4, 9, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto, U.S. Patent 6,288,923 B1, in view of Motomura, U.S. Patent 6,347,055 B1; or alternatively over Taylor et al., U.S. Patent 6,263,398 B1, in view of Motomura, U.S. Patent 6,347,055 B1.

21. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto, U.S. Patent 6,288,923 B1, in view of the admitted prior art, and further in view of Motomura, U.S. Patent 6,347,055 B1.

22. As to claims 4, 9, 14, and 20, none of Sakamoto, Taylor, or the admitted prior art disclose cache holding no more than sixteen addresses. However, an artisan would have recognized the trade-offs between cache size and chip real estate. Motomura teaches an analogous memory integrated

with line buffer circuit which holds no more than sixteen addresses (see Figures 1, 5). The line buffers are analogous to a cache because they are used to improve performance, and include cache characteristics including hit/miss and associativity (see column 1 lines 10-12, and column 8 lines 1-14). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use a cache holding no more than sixteen addresses, because this was a known configuration to achieve a desired price-performance compromise.

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patent No.

5,926,839 Integrated memory and buffer with burst.

5,875,451 Hybrid memory and cache device.

"10ns EDRAM Product Addendum", Enhanced Memory Systems Inc., 1997. EDRAM having DRAM and SRAM on chip, with burst capability.

24. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in Abandonment of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

25. Any inquiry concerning this communication from the examiner should be directed to Gary J. Portka at telephone number (703) 305-4033. The examiner can normally be reached on weekdays from 9:00 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Yoo, can be reached at (703) 308-4908.

Any response to this action should be mailed to (or faxed as provided below):

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Fourth Floor (Receptionist).

The fax phone number for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final communications)

(703) 746-7239 (Official communications)

(703) 746-7240 (Status inquiries, draft communications)

Any inquiry of a general nature relating to this application or proceeding should be directed to the Group receptionist, whose telephone number is (703) 305-3900.

Gary J. Portka

Patent Examiner

September 5, 2002